IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Brahmadathan et al. Confirmation No.: Unknown

Serial No.: Unknown Group Art Unit: Unknown

Filed: Herewith Examiner: Unknown

Title: METHOD, SYSTEM AND PROGRAM PRODUCT FOR AUTONOMOUS ERROR RECOVERY FOR MEMORY DEVICES

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

STATEMENT OF RELEVANCE FOR INFORMATION DISCLOSED BY APPLICANT

Sir:

The following Statement of Relevance is submitted with the accompanying Information Disclosure Citation form.

Document Designation	Relevance
AL	Discloses a method of error recovery processing for a data processor that utilizes parity checking to detect errors.
AM	Discloses a method and system for error recovery for a disk storage system that applies a parity check to data updates.

Full text copies of the art cited, or the pertinent portions thereof, are enclosed. It is respectfully requested that this art be considered by the Examiner in the above-entitled application and made of record therein. The information provided and references enclosed herewith shall not be construed as a representation that a search has been made or that no other art than that identified exists.

Respectfully submitted,

April 01, 2003
Date

Kevin P. Radigan
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INFORMATION DISCLOSURE CITATION (*USE SEVERAL SHEETS IF NECESSARY*)	ATTY DOCKET NO. POU920040034US1	SERIAL NO. UNKNOWN
	APPLICANT(S) **BRAHMADATHAN ET AL.**	
	FILING DATE HEREWITH	GROUP UNKNOWN

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA	4,860,192	08/22/89	Sachs et al.	364	200	
	AB	5,455,939	10/03/95	Rankin et al.	395	182.04	
	AC	5,784,394	07/21/98	Alvarez, II et al.	371	49.1	
	AD	5,883,904	03/16/99	Arimilli et al.	371	10.2	
	AE	5,912,906	06/15/99	Wu et al.	371	40.11	
	AF	6,108,753	08/22/00	Bossen et al.	711	118	
	AG	6,163,857	12/19/00	Meaney et al.	714	7	
	AH	6,199,118 B1	03/06/01	Chin et al.	710	1	
	AI	6,223,655 B1	05/01/01	Shanbaum et al.	101	395	
	AJ	6,332,181 B1	12/18/01	Bossen et al.	711	155	
	AK	6,571,317 B2	05/27/03	Supnet	711	133	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION		
							NO	YES	ABSTRACT
	AL	JP 62260249A	11/12/87	JP	G06F	12/14	X		Yes
	AM	JP 9282105A	10/31/97	JP	G06F	3/06	X		Yes

OTHER DOCUMENTS (*Including Author, Title, Date, Pertinent Pages, Etc.*)

	AN	"Improved Memory Multi-Bit Recovery Algorithm", IBM Technical Disclosure Bulletin, Vol. 34, No. 3, August, 1991.
	AO	"Nonvolatile Write Cache Error Correction", IBM Technical Disclosure Bulletin, Vo. 38, No. 4, April 1995.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial here if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. **Include copy of this form with next communication to applicant.**